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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,851	03/31/2005	Katsumi Suemitsu	8022-1094	1541

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EXAMINER	
VALENTINE, JAMI M	
ART UNIT	**PAPER NUMBER**
2894	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,851	SUEMITSU ET AL.	
	Examiner	Art Unit	
	JAMI M. VALENTINE	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *18 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Application

1. Acknowledgement is made of the amendment received 11/18/08. **Claims 1 and 3-25** are pending in this application. Claims 9 and 19 were amended and claims 21-25 were newly presented in the amendment received 11/18/08.

RCE Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/18/08 has been entered.

Priority

3. The certified English translation of the foreign application has been entered. The application has received the benefit of foreign priority under 35 U.S.C. 119(a)-(d)

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 1, 3, 5- 6 and 11-16** are rejected under 35 U.S.C. 102(b) as being anticipated by Gallagher et al. (US Patent No 5,650,958) hereinafter referred to as Gallagher.

6. Per **Claim 1** Gallagher (e.g. figure 8D) discloses a magnetic memory device, including

- a substrate;(9)

- a lower portion structure (including (12), (14), (16) and (18)) provided on or above said substrate as a portion of a magnetic element; said lower portion structure of said magnetic element comprising a first magnetic film (e.g. (14) or (18))
- an upper portion structure (including (32) (34) and (90)) provided on said lower portion structure of said magnetic element, said upper portion structure of said magnetic element comprising a second magnetic film (32)
- a sidewall insulating film (90) provided to surround said upper portion structure of said magnetic element
- wherein the lower portion structure has an outer circumference that is the same as an outer circumference of a bottom of the sidewall insulating film. (e.g. fig 8D)

7. Per **Claim 3** Gallagher (figure 8D) discloses the device of claim 1, including where said lower portion structure of said magnetic element further comprises a conductive portion (12), the first magnetic film (e.g. (14) or (18)) being provided on or above said conductive portion, and said upper portion structure of said magnetic element comprises an insulating film (20), the second magnetic film (32) being provided on said insulating film (20)

8. Per **Claim 5** Gallagher discloses the device of claim 1, including where said upper portion structure of said magnetic element comprises a conductive film (34) formed on said second magnetic film (32)

9. Per **Claim 6** Gallagher discloses the device of claim 1, including where a plane shape of said upper portion structure of said magnetic element is a rectangle. (column 11 lines 65-67)

10. Per **Claim 11** Gallagher discloses the device of claim 1, including where said sidewall insulating film (40) comprises at least one of silicon oxide, silicon nitride, aluminum oxide, and

aluminum nitride. (column 5 lines 8-9)

11. Per **Claim 12** Gallagher (figures 8A-H) discloses method of manufacturing a magnetic memory device, including

- forming a multi-layer film included in a magnetic element on or above a substrate; (column 9 lines 34-36, see figure 8A)
- etching said multi-layer film into a predetermined pattern up to a predetermined depth, to form an upper portion structure of said magnetic element; (column 10 lines 1-14, see figure 8B-C)
- forming a sidewall insulating film to surround said upper portion structure of said magnetic element; (column 10 lines 23-26, see figure 8D)
- etching a remaining portion of the multi-layer film by using the sidewall insulting film and said upper portion structure of said magnetic element as a mask to form a lower portion structure of the magnetic element. (column 10 lines 23-26, see figure 8D)

12. Per **Claim 13** Gallagher discloses the device of claim 12, including where forming a multi-layer comprises:

- forming a conductive film (12) and a first magnetic layer (14) formed on or above said conductive film in a portion corresponding to said lower portion structure of said magnetic element;
- forming an insulting layer (20) and a second magnetic layer (32) formed on or above said insulating layer in a portion corresponding to said upper portion structure of said magnetic element.

13. Per **Claim 14** Gallagher discloses the device of claim 12, including where said etching said multi-layer film into a predetermined pattern, comprises: etching said multi-layer film into said predetermined pattern by using a physical etching. (Ar+ ion milling, column 10 lines 1-14)

14. Per **Claim 15** Gallagher discloses the device of claim 14, including where said physical etching is ion milling. (Ar+ ion milling, column 10 lines 1-14)

15. Per **Claim 16** Gallagher discloses the device of claim 12, including where forming a multi-layer comprises:

- forming a conductive film (12) in a portion corresponding to said lower portion structure of said magnetic element; and
- forming a first magnetic layer (18) an insulating layer (20) formed on or above said first magnetic layer; and a second magnetic layer (32) formed on or above said insulating layer in a portion corresponding to said upper portion structure of said magnetic element.

16. **Claims 1, 3-5, 8-14, 16, 19 and 21-25**are rejected under 35 U.S.C. 102(e) as being anticipated by Okazawa et al. (US Patent No 2002/0146851) hereinafter referred to as Okazawa.

17. Per **Claims 1 and 10-11** Okazawa (e.g. figure 2J) discloses a magnetic memory device, including

- a substrate (21)
- a lower portion structure (including (23') and (24')) provided on or above said substrate as a portion of a magnetic element; said lower portion structure of said magnetic element comprising a first magnetic film (24').
- an upper portion structure (including ((25'), (26') and (30')) provided on said lower

portion structure of said magnetic element, said upper portion structure of said magnetic element comprising a second magnetic film (26')

- a sidewall insulating film ((31') silicon oxide, see [0057]) provided to surround said upper portion structure of said magnetic element
- wherein the lower portion structure has an outer circumference that is the same as an outer circumference of a bottom of the sidewall insulating film. (e.g. fig 2J)

18. Per **Claim 3** Okazawa discloses the device of claim 1 including where the lower portion structure of said magnetic element further comprises a conductive portion (23'), the first magnetic film being provided on or above said conductive portion, (e.g. figure 2J) and said upper portion structure of said magnetic element comprises an insulating film (25'), the second magnetic film (26') being provided on said insulating film.

19. Per **Claim 4** Okazawa (e.g. figure 2J) discloses a magnetic memory device, including

- a substrate (21)
- a lower portion structure (23') provided on or above said substrate as a portion of a magnetic element; said lower portion structure of said magnetic element comprising a conductive portion (23')
- an upper portion structure (including (24'), (25'), (26') and (30')) provided on said lower portion structure of said magnetic element, said upper portion structure of said magnetic element comprising a first magnetic film (24'), and insulating film (25') formed on or above the first magnetic film (24'), and a second magnetic film (26') formed on or above the insulating film (25')
- a sidewall insulating film (31') provided to surround said upper portion structure of said

first magnetic film (e.g. figure 2J)

- wherein the lower portion structure has an outer circumference that is the same as an outer circumference of a bottom of the sidewall insulating film. (e.g. fig 2J)

20. Per **Claim 5** Okazawa discloses the device of claim 1 including where the upper portion further comprises a conductive film (30') formed on said second magnetic film (26').

21. Per **Claim 8** Okazawa discloses the device of claim 1 including an interlayer insulating film ((33) and (34)) formed to cover said lower portion structure of said magnetic element, said sidewall insulating film, and said upper portion structure of said magnetic element,(figure 2K-L) said interlayer insulating film has a via-contact (see figure 2M-N) connected with said upper portion structure of said magnetic element, and said sidewall insulating film (Silicon Oxide, [0057] is formed of a material which has an etching selection ratio smaller than said interlayer insulating film ((34) is resist which has an etching selection ratio smaller than silicon oxide).

22. Per **Claim 9** Okazawa discloses the device of claim 1 including an interlayer insulating film ((33) and (34)) formed to cover said lower portion structure of said magnetic element, said sidewall insulating film,(figure 2K-L).

23. Per **Claim 12** Okazawa (figures 2A-J) discloses method of manufacturing a magnetic memory device, including

- forming a multi-layer film included in a magnetic element on or above a substrate; (figures 2A-C)
- etching said multi-layer film into a predetermined pattern up to a predetermined depth, to form an upper portion structure of said magnetic element; (figures 2D-E)
- forming a sidewall insulating film ((31) and (32)) to surround said upper portion

structure of said magnetic element; (figures 2F-G)

- etching a remaining portion of the multi-layer film by using the sidewall insulting film and said upper portion structure of said magnetic element as a mask to form a lower portion structure of the magnetic element. (figures 2H-J)

24. Per **Claim 13** Okazawa discloses the method of claim 12, including where forming a multi-layer comprises:

- forming a conductive film (23') and a first magnetic layer (24') formed on or above said conductive film in a portion corresponding to said lower portion structure of said magnetic element; (see figure 2J)
- forming an insulting layer (25') and a second magnetic layer (26') formed on or above said insulating layer in a portion corresponding to said upper portion structure of said magnetic element. (see figure 2J)

25. Per **Claim 14** Okazawa discloses the method of claim 12, including where said etching said multi-layer film into a predetermined pattern, comprises: etching said multi-layer film into said predetermined pattern by using a physical etching. (etched using O_2 plasma [0055])

26. Per **Claim 16** Okazawa discloses the method of claim 12, including where forming a multi-layer comprises:

- forming a conductive film (23') in a portion corresponding to said lower portion structure of said magnetic element; (see figure 2J)
- forming a first magnetic layer (24') an insulating layer (25') formed on or above said first magnetic layer; and a second magnetic layer (26') formed on or above said insulating layer in a portion corresponding to said upper portion structure of

said magnetic element. (see figure 2J)

27. Per **Claim 19** Okazawa discloses the method of claim 12, including forming an interlayer insulating film ((33) and (34)) to cover said lower portion structure of said magnetic element, and said upper portion structure of said magnetic element. (figure 2K-L).

28. Per **Claim 21** Okazawa discloses the device of claim 9 including where the sidewall insulating film (Silicon Oxide, [0057] is formed of a material which has an etching selection ratio smaller than said interlayer insulating film ((34) is resist which has an etching selection ratio smaller than silicon oxide).

29. Per **Claim 22** Okazawa discloses the method of claim 19 including forming a via hole (figures 2M-N) in said interlayer insulating film so as to be connected with said upper portion structure of said magnetic element by an etching method [0060].

30. Per **Claim 23** Okazawa discloses the method of claim 22 including where the sidewall insulating film (Silicon Oxide, [0057] is formed of a material which has an etching selection ratio smaller than said interlayer insulating film ((34) is resist which has an etching selection ratio smaller than silicon oxide).

31. Per **Claim 24** Okazawa discloses the device of claim 1 including a wiring layer (36) arranged to be in electrical contact with an upper surface of the upper portion (figure 2N)

32. Per **Claim 25** Okazawa discloses the method of claim 12 including the step of with the sidewall insulating film in place, forming a wiring layer (36) arranged to be in electrical contact with an upper surface of the upper portion (figure 2N).

Claim Rejections - 35 USC § 103

33. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher in view of Bhattacharyya et al. (US Patent No 6,297,983).

34. Per **Claim 7**, Gallagher discloses the magnetic memory device of claim 1 including and upper and lower portions on a magnetic element.

35. Gallagher does not disclose where a distance d on a plane between an the outer circumference the top of the lower portion structure and an outer circumference of an top of the upper portion structure of said magnetic element has a relation of $0.01\ \mu m \leq d \leq 0.2\ \mu m$

36. Bhattacharyya teaches a magnetic memory device with an upper and lower portion including where a distance c on a plane between an the outer circumference the top of the lower portion structure and an outer circumference of an top of the upper portion structure of said magnetic element has a relation of $0.01\ \mu m \leq d \leq 0.5\ \mu m$. (see figure 6D below, and column 3 lines 62-65)

37. It would have been obvious for one having ordinary skill in the art at the time the invention was made to form the magnetic memory device such that the difference, d, in the outer diamters of the upper and lower portions of the device have the relation $0.01\ \mu m \leq d \leq 0.5\ \mu m$ as taught by Bhattacharyya for the device of Gallagher, in order to minimize the demagnetizing effects emanating from the edges of the magnetic layers in the device. (column 2 lines 61-63)

38. **Claim 17-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher in view of Yoshida et al. (US Patent No 4,566,941).

39. Per **Claim 17**, Gallagher discloses the magnetic memory device of claim 16 including the etching of the multilayer film.

40. Gallagher does not disclose where each of said etching of a remaining portion of said multi-layer film is carried out by using a physical and chemical etching

41. Yoshida teaches the etching of a multilayer film using reactive ion etching, which is both a physical and a chemical etching method. (column 7 lines 11-14)

42. It would have been obvious for one having ordinary skill in the art at the time the invention was made to using a physical and chemical etching method to etch the multilayer film as taught by Yoshida for the device of Gallagher, since reactive ion etching method offers the advantage that an object body can be subjected to anisotropic etching without destroying a thin insulation layer included in said object body. (column 7 lines 11-14)

43. Per **Claim 18**, in so far as definite, the claim is rejected over prior art as follows: Gallagher discloses the magnetic memory device of claim 16 including the etching of the multilayer film.

44. Gallagher does not disclose where each of said etching of a remaining portion of said physical and chemical etching is a reactive ion etching.

45. Yoshida teaches the etching of a multilayer film using reactive ion etching, which is both a physical and a chemical etching method. (column 7 lines 11-14)

46. It would have been obvious for one having ordinary skill in the art at the time the invention was made to using a physical and chemical etching method to etch the multilayer film as taught by Yoshida for the device of Gallagher, since reactive ion etching method offers the advantage that an object body can be subjected to anisotropic etching without destroying a thin insulation layer included in said object body. (column 7 lines 11-14)

47. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa in view

of Tuttle (US Patent No 6,417,561).

48. Per **Claim 20**, Okazawa (figure 2J-M) teaches the device of claim 12, but does not teach the flattening said interlayer insulating film by a chemical mechanical polishing method or an etching-back method.

49. Tuttle teaches planarization of the top surface of an MRAM device by chemical mechanical polishing. (column 7 lines 51-55)

50. It would have been obvious for one having ordinary skill in the art at the time the invention was made to include an interlayer insulating film to cover the upper and lower portions structure of the magnetic element, as well as the sidewall insulating film, and to flatten the interlayer insulating film on said upper portion structure of said magnetic element by a chemical mechanical polishing method, where said sidewall insulating film is formed of a material which has a selection ratio in the chemical mechanical polishing method or the etching-back method smaller than said interlayer insulating film as taught by Okazawa and Tuttle in order provide a flat topography. Planarization of the uppermost layers of such devices was a well known technique at the time the invention was made.

Response to Arguments

51. Applicant's arguments filed 11/18/08 have been fully considered but they are not persuasive.

52. Applicant argues (page 10-11) that the device of Gallagher is not a magnetic memory because the cited figure shows an interim step in the manufacturing process. The examiner respectfully disagrees. The argument is not persuasive because the intermediate device of Gallagher does comprise sufficient structure to function as a magnetic memory. Additionally,

the recitation " a magnetic memory" occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Applicant argues (page 10) that there isn't "any possible way to make electrical contact with the electrode stack. The examiner notes that electrical contact could be made through the sidewalls of any of layers 12, 14, 16, for example. Further, the structure of the device anticipates applicants *claimed* invention. Applicants arguemtns are not evidence, nor are they persuasive.

53. Applicant argues (page 11-12) that Gallagher element (90) is not a sidewall insulating film. This argument is not persuasive. The film (90) is located on the sidewalls of the device and is made from an insulating film. The fact that the applied prior art is an intermediate structure does not negate the fact that the structure meets the recited claim limitations.

54. Applicant's arguments with respect to the previously indicated allowable subject matter are moot since the claims were amended and now stand rejected under a new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMI M. VALENTINE whose telephone number is (571)272-9786. The examiner can normally be reached on Monday-Friday 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jami M. Valentine/
Examiner
Art Unit 2894

/Kimberly D Nguyen/
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